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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/702,320	10/31/2000	Laurence R. Simar, Jr.	TI-30559	9784

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/702,320	SIMAR, JR. ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1* is/are allowed.

6)☒ Claim(s) *7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 7 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 5/23/2005.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Withdrawn Rejections

4. After further consideration, the examiner has withdrawn the 112 rejection set forth in the previous Office Action.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Simar et al., European Patent Application, EP 0855648A2 (as applied in the previous Office Action and

herein referred to as Simar) in view of Hull et al., U.S. Patent No. 5,922,065 (as previously disclosed and herein referred to as Hull), and further in view of Heishi et al., U.S. Patent No. 6,324,639 (as applied in the previous Office Action and herein referred to as Heishi).

7. Referring to claim 7, Simar has taught a method of operating a digital system having a microprocessor (Fig.1, component 11), wherein the microprocessor has a plurality of functional units (Fig.24) for executing instructions in parallel, comprising the steps of:

a) storing fixed and equal length instructions at sequential memory address locations, each instruction including an instruction type and a predetermined p-bit, said p-bit having a first digital state indicating a next instruction is to execute in parallel with said instruction and a second digital state indicating a next instruction is to execute in a cycle after said instruction. See Fig.3 and note that instructions A, B, C, and D, were stored at sequential memory locations x00, x01, x10, and x11. Also, note that in addition to each instruction inherently including an instruction type, each instruction also includes a p-bit with the aforementioned digital states. See Fig.3 and page 3, lines 19-30.

b) fetching a sequence of instruction fetch packets, wherein each fetch packet contains a first plurality of instructions. See Fig.24, packets 1710, 1720, 1730, and 1740. Note that the system will fetch a sequence of instruction packets that contain a first plurality of instructions (in this case the first plurality = 8).

c) scanning the p-bit of each instruction of each fetch packet from lowest memory address location to highest memory address location to determine an execute packet dependent on the p-bits. See Fig.3, page 3, lines 19-30, and page 5, line 54, to page 6, line 7. Note that the fetch packet comprises 4 instructions (A, B, C, and D) and that different size execution packets are

formed based on the values of the p-bits. See Fig.8-19. For example, in Fig.14, instructions are read from lower memory address to higher memory address (as shown in Fig.3), starting with instruction A. Instruction A is added to the execute packet and instruction A's p-bit is checked and determined to be 1. Therefore, this p-bit value indicates that the next instruction (instruction B), may execute in parallel with instruction A. As a result, instruction B is added to the execute packet. Instruction B's p-bit is 0, which means that instruction C must start a new execute packet since it may not execute in parallel with instruction B. The final execute packets are then shown in Fig.15 (note that instructions A and B are in the same packet and C is in its own packet).

d) Simar has not taught scanning the p-bit of each instruction of each fetch packet from lowest memory address location in a first memory fetch packet to highest memory address location in a second immediately following fetch packet to determine an execute packet dependent on the p-bits. However, Hull has taught the concept of executing, in parallel, instructions from multiple fetch packets based on scanning a value of a stop bit. See Fig.3 and Fig.4 and column 3, line 61, to column 4, line 19. Such a bit allows for the definition of inter-bundle (inter fetch packet) boundaries to be defined, which is an extremely valuable processor function. See column 4, lines 55-60. Plus, such combining of fetch packets would maximize processor efficiency. For example, looking at Fig.4, assume that the processor is to first execute a bundle having a template value of 1 and then execute a bundle having a template value of 2. The double lines 42 in the first bundle means that the slot 2 instruction cannot be executed with the slot 0 or slot 1 instruction due to an intra-packet boundary (based on dependencies). Therefore, without the combining of multiple fetch packets, in cycle 0, the slot 0 and slot 1 instructions will execute. In

cycle 1, the slot 2 instruction will execute. On the other hand, with the combining of packets based on a stop bit indicating no inter-bundle boundaries, in cycle 0, the slot 0 and slot 1 instructions will execute. However, this time, in cycle 1, instead of just one instruction (slot 2 instruction) executing, the slot 2 instruction along with instructions from the second bundle will execute. Therefore, more instructions may be executed per cycle when fetch packets may be combined. As a result, it would have been obvious to one of ordinary skill in the art of the invention to modify Simar to include inter-packet combining as taught by Hull.

e) dispatching each instruction within the determined execute packet to one of a second plurality of execution units dependent upon an instruction type of the instruction. See page 3, lines 45-47, of Simar. Note that instructions A and B are executed in parallel, and for them to be executed they must be dispatched to the execution (functional) units in a manner similar to that shown in Fig.24. For instance, if instruction A is an addition-type instruction and instruction B is a multiply-type instruction, then instruction A will be dispatched to the L1 execution unit, since the L1 unit is an arithmetic logic unit, and instruction B will be dispatched to the M1 execution unit since M1 is a multiplier unit (page 4, lines 14-16).

f) Simar has further taught that said step of determining an execute packet boundary dependent upon the p-bits includes:

f1) storing each instruction of said first fetch packet and said second fetch packet. See Fig.24, and note that multiple fetch packets are brought within the system for processing. Simar has not explicitly taught that each instruction of the first and second fetch packets is actually stored in corresponding sections of a first and second latch, respectively. However, Heishi has taught the concept of having two latches and storing two separate fetch packets in them. See

Fig.8, components 221 and 222. Also, see Fig.9B and 9C and note that a first packet comprising units 1, 2, and 3 are stored in the first latch, and units 4, 5, and 6 are stored in a second latch. These units can correspond to short instructions as shown in Fig.18. A person of ordinary skill in the art would have recognized that, in general, it is more efficient to store fetch packets internally (in a latch, cache, etc.) so that a slow main memory access is not required. Having these latches will also mask the main memory access time. For instance, when one packet is being dispatched, no other packet can be dispatched. Therefore, a next packet can be retrieved from memory as opposed to just waiting until the dispatch finishes and then performing the main memory access. By overlapping (pipelining) the main memory access and dispatching, the system becomes more efficient in that when the dispatch does finish, instead of going to slow memory to get the next packet, the packet is retrieved from within the system which is much faster. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Simar in view of Heishi such that first and second fetch packets are store in first and second latches, respectively.

f2) Simar in view of Heishi has further taught selecting only either an entire instruction from a predetermined section of said first latch, an entire instruction from a corresponding section of said second latch, or no instruction, dependent upon only said p-bit from each instruction stored in said first latch and each instruction stored in said second latch. See Fig.24 of Simar, for instance, and note that instructions are selected from the fetch packet, which would be stored in a latch, according to Heishi. This would also hold true for the second fetch packet (for instance, packet 1720 shown in Fig.24 of Simar). Looking at Heishi's dispatch circuitry in Fig.8, an entire instruction will be selected by multiplexer 224b if a corresponding p-bit indicates

that the entire instruction is able to issue in parallel with other instructions in the current cycle. It should be realized that applicant has used alternative language (selecting instruction A, instruction B, or no instruction). Consequently, the prior art of record merely has to select one of the possibilities in order to read on applicant's claim. In this case, an entire instruction is selected from the first latch when a p-bit indicates it is to execute in parallel in the current cycle. It can be seen from Fig.9D, for instance, that mux 224b only selects the entire instruction (unit 3) in the first latch.

Response to Arguments

8. Applicant's arguments filed on May 23, 2005, have been fully considered but they are not persuasive.

9. Applicant argues the novelty/rejection of claim 7 on page 7 of the remarks, in substance that:

> "The combination of Simar and Heishi fails to make obvious the multiplexer selection of no instruction."

10. These arguments are not found persuasive for the following reasons:

a) The examiner asserts that Simar and Heishi are not required to teach such selection of no instruction due to applicant's use of alternative language (select only instruction A, instruction B, or no instruction). Therefore, if the prior art selects just one of the claim options, then the prior art reads on applicant's claim. It should be noted that the examined is not conceding that selection of no instruction is not taught by the prior art. However, the claim does not require such selection.

11. Applicant argues the novelty/rejection of claim 7 on pages 9-10 of the remarks, in substance that:

> "...This teaching of Heishi is contrary to the above quoted recitations of claim 7 which dispatches instruction to a functional unit "dependent upon an instruction type of the instruction." Accordingly, claim 7 is not made obvious by the combination of Simar and Heishi."

12. These arguments are not found persuasive for the following reasons:

a) It should be noted that the primary reference in the combination is the Simar reference, which was relied upon to show the general idea of dispatching. See page 8(e) of the previous Office Action. It was shown that Simar has taught dispatching instructions to units based on instruction type (for instance, a multiply instruction goes to a multiply unit). Heishi was not used to show such a feature. Heishi was used to show storing instructions in latches and their selection for dispatch.

Allowable Subject Matter

13. Claim 1 is allowed.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
July 25, 2005

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